

*via the 1st + 2nd serial links*

second integrated circuit without using caching.

- A1
2. The system of claim 1 wherein the first integrated circuit chip is an application specific integrated circuit (ASIC) chip.
  3. The system of claim 2 7 wherein said first interface is adapted to send a tag to the second interface indicative of a bus transaction type.
  4. The system of claim 2 1 wherein the second integrated circuit chip is adapted configured to enable the transfer of data to the first integrated circuit chip without using caching eashing.
  5. The system of claim 1 further comprising a primary bus coupled to the first integrated chip.  
An interface, comprising:  
an interface adapted to interface parallel data from a parallel data bus to a first bus; and  
a module adapted to interface the parallel data from the parallel data bus into serial data adapted to interface with a second remote bus, the module converting the parallel data to the serial data without using caching.
  6. ~~Delete The system of claim 1 further comprising a secondary bus coupled to the second integrated chip.~~
  7. The system of claim 5 1 further comprising a first interface coupled between the primary bus and the first register and the second register, the first interface configured to determine if a pending address provided thereto represents a transaction to be communicated to the second integrated circuit.
  8. The system of claim 6 7 further comprising a second interface coupled between the secondary bus and the third register and the fourth register.